REMARKS

Claims 1-20 are pending in this application. By this Amendment, claims 1 and 2 are amended to address Yoshimura.

No new matter is added by this Amendment. Support for amendments to claims 1 and 2 can be found at, for example, paragraph [0099] of the specification, describing that the optical wave-guide member forming the optical wave-guide 30 is formed to cover at least the light emitting part 21a of the first micro tile element 21 and the light receiving part 22b of the second micro tile element 22.

I. Allowable Subject Matter

Applicant notes with appreciation that claims 15, 16 and 18 were indicated to be allowable.

II. Rejection Under 35 U.S.C. §102(e)

Claims 1-14, 17, 19 and 20 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,611,635 ("Yoshimura"). This rejection is respectfully traversed.

Claim 1, as amended, recites an optical interconnection circuit between chips having a substrate, a first element having a light emitting function provided on the substrate by an adhesive, a second element having a light receiving function provided on the substrate by an adhesive, an optical wave-guide that optically connects the first element and the second element with each other, and that includes an optical wave-guide member formed on the substrate, the optical wave-guide being in contact with and covering at least a part of a light receiving part of the second element, and an electrode provided on the substrate and connected to at least one of the first element and the second element.

Claim 8 recites an optical interconnection circuit between chips that includes "... a plurality of integrated circuit chips that are mounted onto the substrate, the plurality of

integrated circuit chips including an integrated circuit to time control and an integrated circuit to provide driving, at least one of the plurality of optical wave-guides provided between the integrated circuit to time control and the integrated circuit to provide driving, and the at least one of the plurality of optical wave-guides optically connecting at least one of the plurality of first elements and at least one of the plurality of second elements."

Yoshimura teaches an opto-electronic interconnect substrate 10 that includes a base substrate 12 and an active layer 20. The active layer 20 comprises optical wave-guides 24a-24h, opto-electronic switching devices 26a-26b, photodetector devices 28a-28c, electrical traces 30, and electrical connection pads 32 for the I.C. chips 1. See Yoshimura, column 5, lines 17-29. Yoshimura further teaches that the optical wave-guides 24 and the opto-electronic devices 26 and 28 are incorporated into active layer 20, and are preferably embedded therein such that the top surface of layer 20 is substantially flat. See Yoshimura, column 5, lines 34-37.

Nowhere does Yoshimura teach or suggest an optical wave-guide being in contact with and covering at least a part of a light receiving part of the second element as required in claim 1. In fact, Yoshimura teaches a polishing step that removes the portions of optical wave-guide layer 24 that overlay the opto-electronic components 26 and 28 but maintains the material in the low-lying regions where the optical wave-guides will be defined. Thus, Yoshimura teaches that the wave-guide layer 24 that partially covers the photodetector 28 be removed to make the surface of the substrate more planar. See Yoshimura, column 16, lines 55-63. Clearly, claim 1, as amended, distinguishes over Yoshimura because Yoshimura teaches that the optical wave-guide is not in contact with and does not cover the photodetector 28. Thus, Yoshimura does not teach or suggest the structure of an optical interconnection circuit between chips as recited in claim 1.

Furthermore, nowhere does Yoshimura teach or suggest a plurality of integrated circuit chips including an integrated circuit to time control and an integrated circuit to provide driving and at least one of the plurality of optical wave-guides provided between the integrated circuit to time control and the integrated circuit to provide driving as recited in claim 8. In fact, Yoshimura merely teaches that the optical wave-guides 24a-24h are provided between opto-electronic switching devices 26a-26b and photodetector devices 28a-28c. See Yoshimura, column 6, lines 6-27. Yoshimura further teaches that opto-electronic switching devices 26a-26b and photodetector devices 28a-28c provide the conversions between light and electrical representations of the signals. See Yoshimura, column 5, lines 42-44. Clearly, opto-electronic switching devices 26a-26b and photodetector devices are not integrated circuits that provide either time control or driving. Thus, Yoshimura does not teach or suggest the structure of an optical interconnection circuit between chips as recited in claim 8.

For the foregoing reasons, Yoshimura fails to anticipate claims 1 and 8, and claims dependent therefrom. Reconsideration and withdrawal of this rejection are respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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